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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,263	09/11/2003	Hideto Nakamura	Q77329	3529

7590 05/02/2007

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EXAMINER
SHERMAN, STEPHEN G

ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
05/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/659,263	NAKAMURA ET AL.	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed the 29 March 2007. Claims 1-8 are pending.

Response to Arguments

2. Applicant's arguments with respect to claims 1-6 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saegusa et al. (US 6,175,194) in view of Lim et al. (US 2003/0006945).

Regarding claims 1 and 4, Saegusa et al. disclose a method for driving a display panel in which discharge cells are formed at intersections between a plurality of

row electrode pairs corresponding to display lines, and a plurality of column electrodes intersecting with said row electrode pairs (see col. 1, lines 22-24), said display panel being driven in sub-fields (Fig. 3), each field of a video signal being constituted by a plurality of said sub-fields(Fig. 5), wherein:

each of at least two successive sub-fields (Fig. 5, items SF1 and SF2) including a leading sub-field (Fig. 5, item SF1) includes a selective write addressing step for setting said discharge cells to a lighted discharge cell mode by applying a scan pulse to one row electrode of said row electrode pair while applying a data pulse corresponding to said video signal to said column electrode thereby selectively causing a selective writing discharge in said discharge cells (Fig. 5, see col. 6, lines 47-51, where both SF1 and SF2 contain the step of applying a scan pulse SP to one row electrode while applying a data pulse DP corresponding to said column electrode thereby setting discharge cells to a lighted discharge mode, and thereby causing a writing discharge, by maintaining cells in a lighted discharge mode based on a date pulse of low voltage);

the sub-fields following said at least two sub-fields or leading subfield (Fig. 5, item SF3, of SF2) include a selective erasure addressing step for setting said discharge cells to an unlighted discharge cell mode by applying said scan pulse to one row electrode of said row electrode pair while applying the data pulse corresponding to said video signal to said column electrode thereby selectively causing a selective erasing discharge in said discharge cells (Fig. 5, where SF3 and SF2 contains the step of applying a scan pulse SP to one row electrode while applying a data pulse DP corresponding to said column electrode causing a discharge in said discharge cells, and

this will be an "erasing" discharge when the data pulse is set to not discharge during that subfield);

and an emission sustain step for applying sustain pulses (Fig. 5, items IP) to said row electrode pairs thereby causing a sustain discharge to be repeated a number of times corresponding to a weighting of that sub-field only in said discharge cells that are in said lighted discharge cell mode (Fig. 6, col. 8, lines 38-54, where the weights given to the sustain discharge for each subfield are shown);

the last sub-field of each field (Fig. 6, item SF 14) includes an erasing step for inducing an erasing discharge (Fig. 6, item E) between said column electrode and one of the row electrodes of said row electrode pair belonging to said discharge cells.

Saegusa et al. fail to teach a first erasing step for inducing a first erasing discharge between said column electrode and one of the row electrodes of said row electrode pair in only discharge cells in which both said selective writing discharge and said selective erasing discharge have been caused in each field; and a second erasing step for inducing a second erasing discharge between the row electrodes of said row electrode pair in only discharge cells in which said selective writing discharge has been caused without said selective erasing discharge in each field, said first erasing step and said second erasing step being performed immediately after said emission sustain step.

Lim et al. disclose of a plasma display panel driving method wherein the last subfield includes

a first erasing step for applying a first voltage to one row electrode of said row electrode pair and a second voltage to the other row electrode of said row electrode pair

to induce a first erasing discharge between said column electrode and said one row electrode of said row electrode pair (Figure 7 shows SE1, in which both the Y and Z electrodes have positive voltages applied to them for causing discharge.) in only discharge cells in which both said selective writing discharge and said selective erasing discharge have been caused in each field (Paragraph [0113] explains that the pulses are alternately applied to the Y and Z electrodes for causing discharge within the cells that were not only chosen for selective write, but those that were selected by the selective erasing as described in paragraph [0111].), said first voltage and said second voltage have the same polarity (Figure 7 shows that the voltages are both positive and thus have the same polarity.); and

a second erasing step for inducing a second erasing discharge between the row electrodes of said row electrode pair in only discharge cells in which said selective writing discharge has been caused without said selective erasing discharge in each field (Paragraph [0115] explains that in the last selective erase sub-field discharge is caused in the rest of the cells that are "turned on" by the selective write but we not "turned off" by the selective erase.),

said first erasing step and said second erasing step being performed immediately after said emission sustain step (Figure 7 shows that SE1 and SE2 take place immediately after the sustaining step of the previous sub-field.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Lim et al. in the method of

Saegusa et al. in order to minimize power consumption required for driving the plasma display panel

Regarding claims 2 and 5, Saegusa et al. and Lim et al. disclose the methods for driving a display panel according to claims 1 and 4.

Saegusa et al. further teach the method for driving a display panel further comprising a reset step for initializing all of said discharge cells to said unlighted discharge cell mode (Fig. 6, item Rc, see col. 8, lines 59-61) by causing a universal reset discharge in all discharge cells before said selective write addressing step in only said leading sub-field (see col. 8, lines 59-61).

Regarding claims 3 and 6, Saegusa et al. and Lim et al. disclose the methods for driving a display panel according to claims 1 and 4.

Saegusa et al. further teach the method for driving a display panel wherein intermediate luminance of N+1 gradations (Fig. 6 and Fig. 21, where there are 14 gradations of luminance shown) is displayed by inducing sustain charges (Fig. 6, item Ic, see col. 8, line 30) in said emission sustain steps of N leading sub-fields of each field (In Fig. 6, here N = 13 and there are emission sustain steps shown for sub-fields 1-13).

Regarding claims 7 and 8, Saegusa et al. and Lim et al. disclose the methods for driving a display panel according to claims 1 and 4.

Lim et al. also disclose wherein only said last sub-field of each field includes said first erasing step and aid second erasing step (Figure 10 shows that SE1 and SE2 are both located only after SW1, SW2, etc.).

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

23 April 2007

AMR A. AWAD
SUPERVISORY PATENT EXAMINER